

SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a semiconductor device and a fabrication method thereof, particularly to a SON (Small Outline Non-Lead Package) type semiconductor device and a fabrication method thereof.

Description of the Related Art

A semiconductor device is known in which an external electrode of a semiconductor chip is electrically connected to a conductor terminal with a bonding wire and the semiconductor chip, the bonding wire and the conductor terminal are encapsulated with an insulator.

In the semiconductor device like this, a so-called SON type semiconductor device is known in which a conductor terminal is exposed from an insulator.

Furthermore, in order to reduce the exposure failure of the conductor terminal of the SON type semiconductor device like this, a fabrication process of a conductor terminal is known in which the conductor terminal is formed with the use of a conductor that an adhesion to a substrate is reduced under a predetermined condition and the adhesion between the substrate and the conductor terminal is reduced for removal under a predetermined condition after its encapsulation process step

(for example, see Patent Document 1).

Patent Document 1 JP-A-2003-078076

SUMMARY OF THE INVENTION

In the fabrication process of the traditional SON type semiconductor device like this, a leadframe needs to be prepared with matching to the size of a semiconductor chip or the arrangement of electrode pads formed on the top surface of the semiconductor chip, that is, for every semiconductor chip of particular specifications.

In addition, according to the traditional fabrication process, a dice bonding process step, a wire bonding process step, a resin encapsulation process step, and a separation process step cannot be combined into a series of process steps. Therefore, since semiconductor devices in midstream of fabrication dwell until they are processed by the subsequent process step, the time required to fabricate a semiconductor device is increased.

The invention has been made in view of the problems. In order to solve the problems, a fabrication method of a semiconductor device according to the invention mainly includes the process steps below.

More specifically, first, a plurality of linear leadframes is arranged side by side separately from each other.

Then, a plurality of semiconductor chips having a first

main surface with a plurality of electrode pads and a second main surface facing the first main surface is placed over a plurality of linear leadframes and separated from each other in the direction of extending the linear leadframes with the second main surface of each of the semiconductor chips mounted thereon.

Furthermore, the plurality of the electrode pads is joined to the plurality of the linear leadframes with bonding wires.

Moreover, an encapsulation part for encapsulating the semiconductor chip and the bonding wires and an interframe encapsulation part for burying a space between the adjacent linear leadframes exposed outside the encapsulation part are formed.

Subsequently, a groove part for cutting all the linear leadframes placed right under the second main surface in the vertical direction to the direction of extending the linear leadframes.

After that, the leadframes and the interframe encapsulation parts exposed between the plurality of the semiconductor chips are cut to separate into semiconductor devices having the semiconductor chip and a first external terminal row and a second external terminal row facing each other as sandwich the groove part.

According to the fabrication method of the semiconductor device according to the invention, since the interval between

the leadframes arranged is easily matched to the interval between the external terminals, leadframes do not need to be prepared for every semiconductor chip with particular specifications.

Moreover, the dice bonding process step, the wire bonding process step, the resin encapsulation process step, and the separation process step can be conducted in a series of process steps on the plurality of the leadframes arranged. Therefore, the semiconductor devices in midstream of fabrication do not dwell until they are processed by the subsequent process step.

Accordingly, many semiconductor devices can be fabricated efficiently for a short time. Furthermore, it also contributes to the reduction in the fabrication costs of the semiconductor device.

BRIEF DESCRIPTION OF THE DRAWINGS

The teachings of the invention can be readily understood by considering the following detailed description in conjunction with the accompanying drawings, in which:

Fig. 1 is a schematic diagram for illustrating the outline of a fabrication apparatus for conducting the fabrication method of the semiconductor device according to the invention, and the outline of each of the process steps included in the fabrication method according to the invention;

Figs. 2A to 2D are fabrication process diagrams (No. 1) depicting a semiconductor device of a first embodiment;

Figs. 3A to 3D are fabrication process diagrams (No. 2) depicting the semiconductor device of the first embodiment;

Figs. 4A to 4C are fabrication process diagrams (No. 3) depicting the semiconductor device of the first embodiment;

Figs. 5A to 5C are schematic diagrams depicting the semiconductor device of the first embodiment;

Figs. 6A to 6D are fabrication process diagrams depicting a semiconductor device of a second embodiment; and

Figs. 7A to 7C are schematic diagrams depicting the semiconductor device of the second embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Hereinafter, embodiments according to the invention will be described with reference to the drawings. In addition, the shape, size and arrangement of each component are only shown schematically in the drawings to the extent that the invention is understood, which do not define the invention particularly. Besides, specific materials, conditions and numeric conditions are sometimes used in the description below, but they are merely one of preferable examples. Thus, the invention is not defined by them at all.

Moreover, the fabrication process of the semiconductor device according to the invention can be formed by traditionally well-known fabrication process steps with the use of traditionally well-known materials. Therefore, the detailed

description of the traditionally well-known fabrication process steps might be omitted.

First, an overview of the fabrication method of the semiconductor device according to the invention will be described.

Fig. 1 is a schematic diagram for illustrating the outline of a fabrication apparatus 100 for conducting the fabrication method of the semiconductor device according to the invention, and the outline of each of the process steps included in the fabrication method according to the invention.

A semiconductor device according to the invention is fabricated by the fabrication apparatus 100 having first and second reels 110a and 110b separated in parallel to each other.

More specifically, the fabrication method of the semiconductor device according to the invention is characterized in that all of a dice bonding process step 120, a wire bonding process step 122, an encapsulation process step 124, an external terminal forming process step 126, and a separation process step 128 are conducted on leadframes 12, which will be described below in detail.

Both end parts of the leadframe 12 are extended between first and second reels 110a and 110b, respectively. Furthermore, the both end parts of the leadframe 12 are wound on the two first and second reels 110a and 110b in the reverse directions each other. A plurality of the leadframes 12 is

separated from each other in stripes and extended and held between the two first and second reels 110a and 110b.

In order to prevent the misalignment of the plurality of the leadframes 12, a plurality of grooves (not shown) is preferably formed with matching to the interval between the leadframes 12, and the leadframes 12 are wound in the corresponding grooves..

The dice bonding process step 120, the wire bonding process step 122, the encapsulation process step 124, the external terminal forming process step 126, and the separation process step 128 can be conducted at the same time by rotating the two first and second reels 110a and 110b in the same directions at the same time and moving them sequentially.

First, the dice bonding process step 120 of mounting first semiconductor chips on the leadframes 12 is conducted. Then, the first and second reels 110a and 110b are rotated in the same directions to move a first semiconductor chip by a predetermined distance. The dice bonding process step of mounting a second semiconductor chip on the area generated by the movement is conducted. At this time of the dice bonding process step, the first semiconductor chip moved undergoes the wire bonding process step 122. In this manner, after completion of each process step, the leadframes 12 are sequentially moved in the direction from the first reel 110a to the second reel 110b, the dice bonding process step 120, the wire bonding process

step 122, the encapsulation process step 124, the external terminal forming process step 126, and the separation process step 128 are conducted at the same time.

The leadframes 12 are placed on a platen or table-shaped structure provided for the fabrication apparatus used in each of the process steps for conducting each of the process steps. Furthermore, for example, it is acceptable to conduct each of the process steps as the leadframes 12 are placed on a structure such as a platen that moves as it follows the rotations of the first and second reels 110a and 110b, that is, the movement of the leadframes 12.

Moreover, each of the process steps can be freely conducted to a preferable number of the semiconductor chip, one, two or more. In the example described below, an example that each of the process steps is conducted as two semiconductor chips are one unit will be described.

<First Embodiment>

1-1. Fabrication Method of the Semiconductor Device

The fabrication method of the semiconductor device of the first embodiment according to the invention will be described with reference to Figs. 2A to 4D.

Figs. 2A to 2D are explanatory diagrams (No. 1) for illustrating the fabrication process steps of the semiconductor device of the first embodiment. Fig. 2A is a schematic plan

view for illustrating the fabrication process step of the semiconductor device. Fig. 2B is a schematic diagram depicting a section cut by an alternate long and short dashed line indicated by 2B-2B shown in Fig. 2A. Fig. 2C is a schematic plan view for illustrating the fabrication process step of the semiconductor device. Fig. 2D is a schematic diagram depicting a section cut by an alternate long and short dashed line indicated by 2D-2D shown in Fig. 2C.

Figs. 3A to 3D are explanatory diagrams (No. 2) depicting the fabrication process steps of the semiconductor device of the first embodiment. Fig. 3A is a schematic plan view for illustrating the fabrication process step of the semiconductor device. Fig. 3B is a schematic diagram depicting a section cut by an alternate long and short dashed line indicated by 3B-3B shown in Fig. 3A. Fig. 3C is a schematic plan view for illustrating fabrication process step of the semiconductor device. Fig. 3D is a schematic diagram depicting a section cut by an alternate long and short dashed line indicated by 3D-3D shown in Fig. 3C.

Figs. 4A to 4C are explanatory diagrams (No. 3) depicting the fabrication process steps of the semiconductor device of the first embodiment. Fig. 4A is a schematic plan view for illustrating the fabrication process step of the semiconductor device. Fig. 4B is a schematic diagram depicting a section cut by an alternate long and short dashed line indicated by

4B-4B shown in Fig. 4A. Fig. 4C is a schematic plan view for illustrating the fabrication process step of the semiconductor device.

The leadframe 12 used for the fabrication method according to the invention has a long, linear shape. These leadframes 12 are preferably formed in bands (strips) of a conductive metal material such as copper or a copper alloy. The shorter length (width) is about 0.2 to 0.5 mm, in a typical standard example in the present semiconductor device.

As shown in Fig. 2A, a plurality of the leadframes 12 is separated in stripes at an equal interval d , and is extended and held between the two first and second reels 110a and 110b as described above.

The leadframe 12 functions as the external terminal of the semiconductor device to be fabricated. Therefore, the interval d between the plurality of the leadframes 12 disposed in parallel to each other is determined to be equal to the interval between the external terminals in accordance with the specifications of the semiconductor chip to be mounted on the leadframes 12 and the specifications of the semiconductor device to be fabricated, which will be described later. The interval between the external terminals corresponding to the interval d between the leadframes 12 is about 0.5 to 1.5 mm, in a typical standard example in the present semiconductor device.

Therefore, in this example, the example that the plurality

of the leadframes 12 is arranged at the equal interval d will be described, but it is easy to arrange the leadframes 12 at different intervals in accordance with the specifications of external terminals, for example.

As shown in Fig. 2A, among the plurality of the leadframes 12 arranged side by side, two leadframes 12 placed at the outermost positions are referred to as a first outermost leadframe 12a and a second outermost leadframe 12b, respectively.

As shown in Fig. 2B, one main surface of the leadframe 12 is a front side 12c, and the other main surface is a back side 12d. The front side 12c is also called a top surface, and the back side 12d is also called an under surface. Preferably, palladium is coated over throughout the surface including the top surface 12c and the under surface 12d beforehand by a plating process step according to traditional methods.

Subsequently, as shown in Fig. 2C, semiconductor chips 20 are arranged separately from each other in the direction (long direction) of extending the leadframes 12 so that each of the semiconductor chips 20 is placed over the plurality of the linear leadframes 12.

The semiconductor chip 20 generally has a substantially rectangular parallelepiped. The semiconductor chip 20 has a first main surface 20a with a plurality of electrode pads 22 and a second main surface 20b facing to the first main surface

20a. The first main surface 20a and the second main surface 20b of the semiconductor chip 20 are the same rectangular shape in this example. Furthermore, two end faces 20c and 20c facing each other and two side faces 20d and 20d orthogonal to the end faces 20c and 20c and facing each other are between the first and second main surfaces.

Here, suppose the number of the leadframes 12 is seven and the number of the semiconductor chips 20 to be mounted is two for description.

The semiconductor chip 20 is dice-bonded on the leadframes 12 so that the long direction of the rectangular of the first main surface 20a and the second main surface 20b is orthogonal to the direction of extending the leadframes 12. In this case, the end faces 20c and 20c of the semiconductor chip 20 are along the direction of extending the leadframes 12, and the semiconductor chip 20 is not mounted on the leadframes 12 adjacent to the first and second outermost leadframes 12a and 12b. More specifically, two each of the leadframes 12 including the first and second outermost leadframes 12a and 12b on the outside are exposed from the mounted semiconductor chip 20.

In mounting the semiconductor chip, the second main surface 20b of the semiconductor chip 20 is attached onto the top surfaces 12c of three leadframes 12 in the center through an insulating adhesive 30 (Fig. 2D).

As the insulating adhesive 30, traditionally well-known

products can be preferably used freely. For the adhesive 30, insulating adhesive tapes, for example, are acceptable as well as paste adhesives.

The electrode pads 22 are disposed and exposed on the first main surface 20a. In this example, five each of the plurality of the electrode pads 22 are arranged along two side faces 20d and 20d of the semiconductor chip 20 so that the electrode pads 22 along the same side faces are arranged at equal intervals. Moreover, the electrode pads on each of the side faces 20d and 20d are arranged and faced to each other at equal intervals.

As described above, the interval d between the plurality of the leadframes 12 is determined equal to the interval between the external terminals of the semiconductor chips to be mounted on the leadframes 12 or the semiconductor device to be fabricated. The interval between the external terminals is determined in accordance with the specifications of the semiconductor chip 20 or the semiconductor device 10 to be fabricated.

Then, the electrode pads 22 are joined to five leadframes 12 inside with bonding wires 40 (Figs. 3A and 3B). The bonding process step is freely conducted by preferable methods such as thermocompression bonding and ultrasonic thermocompression bonding with the use of traditionally well-known bonding wires and a bonding apparatus.

At this time, the configuration is fine that the bonding

wires 40 are not joined to the first and second outermost leadframes 12a and 12b. With doing this, it is easy to prevent an encapsulation resin material from leaking over the first and second outermost leadframes 12a and 12b in the encapsulation process step, which will be described later.

The bonding wires 40 are bonded to the leadframes 12 exposed around the semiconductor chip 20. In the exemplary configuration shown in the drawing, a pair of electrode pads 22 on a straight line along the direction of extending a leadframe 12 is joined to the same leadframe 12 among the electrode pads 22 of the semiconductor chip 20.

Subsequently, as shown in Figs. 3C and 3D, an encapsulation part 50 for encapsulating the semiconductor chip 20 and the bonding wires 40 is formed. The appearance of the structure where the encapsulation part 50 is formed is a substantially rectangular parallelepiped. The side faces around the rectangular parallelepiped are encapsulation part side faces 50b and 50b and encapsulation part end faces 50c and 50c.

The encapsulation part 50 can be formed by a traditionally well-known encapsulation process step with a mold, for example, with the use of proper materials such as traditionally well-known molding resins and liquid resins freely. In this example, the encapsulation process step can be conducted by using a traditionally well-known encapsulation apparatus with a mold capable of forming a cavity that can house a single semiconductor

chip bonded on the leadframes 12, for example. More specifically, a cavity to house a single semiconductor chip is formed by an upper mold to surround a single semiconductor chip 20 as contacted with the top surfaces 12c of the leadframes 12 on which the semiconductor chip 20 is mounted and a lower mold contacted with throughout the under surfaces 12d (both molds are not shown). Then, the encapsulation resin material is filled in the cavity and cured to form the encapsulation part 50.

Therefore, the encapsulation part 50 of the semiconductor device 10 of the embodiment is formed so as to package the semiconductor chip 20 one each.

By the encapsulation process step, the spaces between the plurality of the linear leadframes are also buried with the encapsulation resin material to form interframe encapsulation parts 50d. However, at this time, the top surfaces 12c of the leadframes 12 outside the encapsulation part 50 are exposed.

After that, all the leadframes 12 placed right under the second main surface 20b of the semiconductor chip 20 are cut in the vertical direction to the end faces 20c and 20c of the semiconductor device 20, that is, the direction along the side faces 20d and 20d. A groove part 60 is thus formed. This process step can be conducted by using a traditionally well-known dicing apparatus.

As shown in Fig. 4A, in this example, a dicing line A is set beforehand on the second main surface 20b (see Fig. 4B) along the direction orthogonal to the direction of extending the leadframes 12. The dicing line A is a line passing through the center of the width of the second main surface 20b along the direction of extending the leadframes 12. The dicing line A preferably divides the areas of the first and second main surfaces 20a and 20b and the end faces 20c and 20c into two equally.

As shown in Fig. 4B, the groove part 60 is formed along the dicing line A across at least the leadframes 12 on which the second main surface 20b of the semiconductor chip 20 is mounted for cutting them. At this time, the depth (height) of the groove part 60 is determined as the depth that the leadframes 12 can be cut completely and the range that the function of the semiconductor chip 20 is not impaired. Therefore, it is fine that the depth is set to expose the second main surface 20b of the semiconductor chip 20 at the maximum.

In the process step of cutting the leadframes 12, that is, the process step of forming the groove part 60, it is preferable to form the groove part 60 so as not to cut the first and second outermost leadframes 12a and 12b.

With doing this, since the encapsulation resin material is filled between the adjacent leadframes and continues to the outermost leadframes 12a and 12b, the strength of the entire

structure of connecting the semiconductor devices in midstream of fabrication can be secured. Therefore, a plurality of the connected semiconductor devices in midstream of fabrication can be moved easily and sequentially after the completion of the process steps by the first and second outermost leadframes 12a and 12b that are not cut for implementing it in a series of the fabrication process steps, as conducted in the fabrication process of TCP, for example.

After that, as shown in Fig. 4C, each of the semiconductor chips 20 is cut therearound to separate into the semiconductor device 10 including the semiconductor chip 20 (see, Fig. 5A). Also in the separation process step, the first and second outermost leadframes 12a and 12b are not cut.

The separation process step is conducted by pressing molds surrounding the area enclosed by a broken line B shown in Fig. 4C, such as upper and lower molds with the same shapes as those used in the encapsulation process step. Pressing the molds can cut a plurality of the leadframes 12 inside and the interframe encapsulation parts 50d burying the spaces between the leadframes 12.

The separation process step like this is conducted to obtain the semiconductor device 10.

In this manner, according to the fabrication method of the semiconductor device of the invention, since a plurality of the process steps can be conducted on the leadframes 12

continuously, the semiconductor devices in midstream of fabrication do not dwell until they are processed by the subsequent process step before. Accordingly, many semiconductor devices can be fabricated efficiently for a short time. Furthermore, it contributes to the reduction in the fabrication costs of the semiconductor device.

1-2. Semiconductor Device

The configuration of the semiconductor device fabricated by the fabrication method of the first embodiment described with reference to Figs. 2A to 4C will be described with reference to Figs. 5A, 5B and 5C.

Fig. 5A is a schematic perspective view for illustrating the exemplary configuration of the semiconductor device 10 of the first embodiment. Fig. 5B is a schematic diagram depicting a section of the semiconductor device 10 cut by an alternate long and short dashed line indicated by 5B-5B shown in Fig. 5A. Fig. 5C is a plan view depicting the semiconductor device 10 seen from the bottom (external terminal side).

In addition, in the description of the semiconductor device, selection of materials for each component is described already, thus omitting the detailed description.

The semiconductor device 10 fabricated by the fabrication method of the semiconductor device of the first embodiment includes the semiconductor chip 20. As described above, the

semiconductor chip 20 is in a nearly rectangular parallelepiped having the first main surface 20a, the second main surface 20b facing the first main surface 20a, and the end faces 20c and the side faces 20d between the first main surface 20a and the second main surface 20b. The plurality of the electrode pads 22 is exposed from the first main surface 20a. The plurality of the electrode pads 22 is arranged along the side faces 20d on the first main surface 20a (see Fig. 2C).

The semiconductor device 10 includes a plurality of external terminals 14. The external terminals 14 are disposed and attached on the second main surface 20b of the semiconductor chip 20 through the insulating adhesive 30. In this example, the external terminal 14 is formed of the leadframe 12 in a strip. As described above, the interframe encapsulation part 50d is disposed between the side faces of the leadframes 12.

As shown in Fig. 5B, the external terminals 14 are disposed so as to be exposed from the outline of the semiconductor chip 20. More specifically, the external terminals 14 are disposed as a first external terminal row 14X including a plurality of first external terminals 14a. Similarly, a second external terminal row 14Y including a plurality of second external terminals 14b is also disposed on the other side face 20d. In this example, the first external terminal row 14X and the second external terminal row 14Y face each other as sandwich the groove part 60 extending in the vertical direction to the end faces

20c and 20c.

The first and second external terminals 14a and 14b are extended in the vertical direction to the side faces 20d facing each other, respectively, and arranged side by side at a predetermined distance apart in the plane in parallel to the second main surface 20b of the semiconductor chip 20, that is, at equal intervals in this example.

The electrode pads 22 and the external terminals 14 are joined to each other with the bonding wires 40. In this example, the surfaces of the electrode pad 22 and the external terminal 14, that is, front sides 14aa and 14ba are joined in correspondence one for one.

The semiconductor device 10 has the encapsulation part 50 for encapsulating the semiconductor chip 20 and the bonding wires 40 and the interframe encapsulation parts 50d outside the encapsulation part 50. In this example, the encapsulation part 50 is disposed as a shape where a structure of a nearly rectangular parallelepiped is placed on the first and second external terminal rows 14X and 14Y.

The interframe encapsulation parts 50d are disposed so as to bury the spaces between a plurality of the external terminals 14a and between the external terminals 14b as exposed outside the encapsulation part 50. However, the interframe encapsulation parts 50d are disposed so as to expose a part of the front sides 14aa and 14ba and back sides 14ab and 14bb

of the external terminals 14a and 14b.

According to the semiconductor device of the first embodiment, since the external terminals 14 are disposed two-dimensionally as adjoin the second main surface 20b of the semiconductor chip 20, the semiconductor device can be formed in a lower profile, that is, in a smaller shape. Moreover, since the external terminals are exposed widely on the back side, heat generated by the semiconductor chip can be dissipated efficiently.

<Second Embodiment>

2-1. Fabrication Method of the Semiconductor Device

A fabrication method of a semiconductor device of a second embodiment according to the invention will be described with reference to Figs. 6A to 6D. In addition, the differences between the fabrication method of the semiconductor device of the embodiment and the semiconductor device fabricated by the fabrication method and the first embodiment reside in the process step of forming an encapsulation part 50, the shape of the encapsulation part 50, and a separation process step. Thus, they will be described, and the drawings and detailed description of the same process steps and configurations as those in the first embodiment are omitted.

Figs. 6A to 6D are explanatory diagrams depicting the fabrication process steps of the semiconductor device of the

second embodiment. Fig. 6A is a schematic plan view for illustrating the fabrication process step of the semiconductor device, particularly the encapsulation process step. Fig. 6B is a schematic diagram depicting a section cut by an alternate long and short dashed line indicated by 6B-6B shown in Fig. 6A. Fig. 6C is a schematic plan view for illustrating the fabrication process step of the semiconductor device, particularly the separation process step. Fig. 6D is a schematic diagram depicting a section cut by an alternate long and short dashed line indicated by 6D-6D shown in Fig. 6C.

In the fabrication method of the second embodiment, since a dice bonding process step, a wire bonding process step (Figs. 2A to 3B), and an external terminal forming process step (Figs. 4A and 4B) are the same as those in the first embodiment, see the description in the first embodiment.

As shown in Figs. 6A and 6B, an encapsulation layer 70 for encapsulating a semiconductor chip 20 and bonding wires 40 joined to the semiconductor chip is formed.

The encapsulation layer 70 is formed so as to expose first and second outermost leadframes 12a and 12b on end faces 20c and 20c of the semiconductor chip 20 and to cover two or more of the semiconductor chips on side faces 20d and 20d of the semiconductor chip 20, a preferable number is set freely.

The encapsulation process step can be conducted by using the traditionally well-known encapsulation apparatus with the

molds having the structure described on the first embodiment, other than forming a cavity that can house a plurality of the semiconductor chips bonded on leadframes 12, a preferable number is set freely.

As a matter of course, the spaces between the plurality of the linear leadframes are buried with the encapsulation resin material by the encapsulation process step.

Subsequently, all the leadframes 12 placed right under the second main surface 20b of the semiconductor chip 20 are cut at a scribe line A (see Fig. 6C) to form a groove part 60 as similar to the first embodiment.

After that, as shown in Figs. 6C and 6D, the semiconductor device 10 including the semiconductor chip 20 is separated into each piece (see Figs. 6A to 6D) in which the encapsulation layer 70 and the leadframes 12 are cut along scribe lines C extended in the direction orthogonal to the first and second outermost leadframes 12a and 12b and set in the space between the semiconductor chips 20 and scribe lines D extended in the direction along the first and second outermost leadframes 12a and 12b. The difference between the configuration of the semiconductor device 10 thus obtained and that of the semiconductor device described in the first embodiment is in that the semiconductor device of the second embodiment itself is substantially in a nearly rectangular parallelepiped and has no projecting external terminals.

For the separation process step, for example, the traditionally well-known dicing apparatus similar to that used in forming the groove part 60 can be used.

According to the fabrication method of the semiconductor device of the second embodiment, in addition to the advantages obtained by the fabrication method of the first embodiment, the process step of forming the groove part 60 and the separation process step can be conducted by using the same apparatus. Furthermore, the separation process step can be made a simpler process step. Therefore, the semiconductor device can be fabricated more efficiently.

2-2. Semiconductor Device

The configuration of the semiconductor device fabricated by the fabrication method of the second embodiment will be described with reference to Figs. 7A, 7B and 7C.

Fig. 7A is a schematic perspective view for illustrating the exemplary configuration of the semiconductor device 10 of the second embodiment 10. Fig. 7B is a schematic diagram depicting a section of the semiconductor device 10 cut by an alternate long and short dashed line indicated by 7B-7B shown in Fig. 7A. Fig. 7C is a plan view depicting the semiconductor device 10 seen from the bottom (external terminal side).

In addition, the encapsulation part having the configuration different from that of the semiconductor device

of the first embodiment will be described here, and the detailed description of the other same configuration as that of the first embodiment is omitted.

As shown in Figs. 7A and 7B, the encapsulation part 50 is formed in a nearly rectangular parallelepiped. The encapsulation part 50 encapsulates the semiconductor chip 20, the bonding wires 40 and the external terminals 14. The external terminals 14, that is, the first and second external terminals 14a and 14b are disposed so that the sections generated by the separation process step are exposed from both encapsulation part side faces 50b and 50b, respectively.

Moreover, as shown in Figs. 7B and 7C, the encapsulation part 50 is disposed so as to expose back sides 14ab and 14bb thereof.

According to the semiconductor device of the second embodiment, in addition to the advantages obtained by the semiconductor device of the first embodiment, the semiconductor device can be formed further smaller because the external terminals 14 are not projected from the encapsulation part 50.